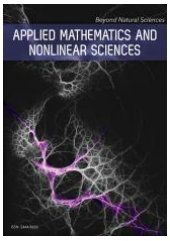
sciendo Applied Mathematics and Nonlinear Sciences, 9(1) (2024) 1-15



Applied Mathematics and Nonlinear Sciences

https://www.sciendo.com

Design of industrial equipment data acquisition system based on ZYNQ

Xiaoping Zhang[1,†], Qingqing Xing[1], Xichen Yu[1], Shili Pan[1]

1. School of Technology, Applied Technology College of Soochow University, Kunshan, Jiangsu, 215300, China.

Submission Info

Communicated by Z. Sabir
Received January 29, 2023
Accepted July 10, 2023
Available online December 30, 2023

Abstract

In this paper, an industrial equipment data acquisition system based on a ZYNQ chip is constructed using an AD7607 data acquisition module containing a symmetric layout. Next, four modules of signal output, data writing, caching and communication are designed. Focusing on the design of the signal processing system after analog-to-digital conversion, the D-S evidence processing algorithm is utilized to judge the obtained data independently and fuse the data based on its D-S combination rule. Finally, the industrial equipment acquisition system design is tested, and the test includes system performance, accuracy, and stability. The frequency peaks obtained by the system in this paper are all 1000.000Hz, as shown by the results. The signal peak value of 95.18mV, the NI acquisition card signal peak value of 98.33mV, and the error is only 0.89%. The signal-to-noise ratio of the sampled signal is 50.12dB, and the effective number of bits reaches 10.40 bits. The performance of the system and the accuracy and stability of data acquisition on industrial equipment are verified.

Keywords: ZYNQ; Data fusion; Data acquisition; Industrial equipment; D-S evidence theory.
AMS 2010 codes: 68P01

†Corresponding author.
Email address: crystalzxp@163.com

ISSN 2444-8656
https://doi.org/10.2478/amns.2023.2.01704

1 Introduction

The rapid development of information technology continues to promote the integration of the Internet and industry, prompting the smart manufacturing industry to enter a new stage [1-2]. China formally introduced the "Made in China 2025" strategy in 2015, aiming to vigorously develop the manufacturing industry to realize a strong manufacturing country [3-4]. One of the important steps is to use a large number of automated industrial equipment to replace human labor, to achieve intelligent and unmanned factories [5]. However, industrial equipment brands are diverse, and each equipment manufacturer independently adopts different communication protocols and specifications, which makes the cost of acquiring equipment data in factories greatly increased [6].

Data acquisition is becoming more and more important as the primary issue of modern industrial information processing [7]. With the improvement of embedded technology, more and more embedded systems are applied in high precision data acquisition systems [8-9]. In the process of practical application, a single FPGA or ARM can not meet the user's needs in some areas, so the ZYNQ series products from Xilinx have been widely considered since their introduction [10-12].

Data acquisition systems play an important role in modern industrial production, scientific experiments and other fields, and these systems can help people better understand the performance and operation of equipment. With the progress of science and technology, the requirements for data acquisition equipment in various industries are getting higher and higher [13]. Literature [14] suggests that today's manufacturers have PLCs, PACs and PCs as many automation controllers and data acquisition options, all of which can be the stable and reliable operation of factory automation equipment and data acquisition. However, in terms of compatibility, size and capacity by the differences, it is necessary to match the most suitable manufacturer of industrial equipment. Literature [15] on intelligent manufacturing of big data analysis to explore, for example, through the analysis of all the data on the factory floor, equipment monitoring data, enterprise manufacturing database, self-learning, decision-making, adaptive to a variety of environments, so that the data can be effectively utilized to improve the production line automation, high efficiency, and stabilization, but also for the intelligent data collection, and the direction of the future development of the equipment to provide a reference. Literature [16] proposed an INTERNET-based human-machine interface to build embedded Visual Studio, and then FPRS control over the basic principles of communication systems to create an application server protocol, the development of the completed software on the DCM torque, speed, power, etc., detection, the design makes low-cost real-time monitoring can be realized. Literature [17] for the unmanned management of power grids, build a structured system based on the Internet of Things technology of the Internet of Things monitoring network of electric power equipment, combined with image recognition data and collect, fill the gaps in the data, analyze the data, look at the loss of to the control side, relying on the LPWAN to achieve remote monitoring.

After simulation experiments, the research results show that real-time unmanned monitoring is achieved, providing a reference for the future operation and maintenance of power grid equipment. Literature [18] uses Cloud Advanced Metering Infrastructure (CAMI) with Zynq UltraScale+ device Field Programmable Gate Array (FPGA), comparing with existing Digital Signal Processing (DSM) systems, which uses DSM driven by accurate transcription and encryption to serve end-users. Literature [19] describes the data collection for a high particle-strength analog thermon calorimeter at the future International Linear Collider, focusing on the central ZYNQ-Sysem-On-Chip to demonstrate in detail the high performance and stability of this data collection system. Literature [20] describes the ZYNQ system-on-chip SOC as a widely used architecture based on which a model for parameter extraction is given. Optimize the implementation of algorithms PSO and SIMKIT, the first PSO algorithm running on PL, pup PSP MOSFET library SIMKIT implemented on PS, the

experimental results show that, compared to ARM, PSO implementation efficiency increased significantly, dual-core again than a single-core performance by one-quarter.

In this paper, the Zynq-7010 platform is used as the basic hardware equipment of the information acquisition system, and the AD7607 module is used to form the AN706 module, which in turn is used to form the industrial equipment acquisition system module. Secondly, the software design is divided into five modules, namely, the industrial data acquisition module, the data output function module for waveform data generation, the control module of the data in the FPGA underlying program, the data cache module written from the outside, and the PL-PS communication interface module. In the process of processing and analyzing the collected data, this paper adopts the data fusion technique based on the D-S evidence theory and performs the synthesis operation of multiple D-S to make up for the shortcomings of uncertainty when dealing with a single piece of evidence by this technique. Finally, three groups of experiments are designed. One group tests the overall power consumption of the system in normal operating mode, idle mode, and dormant mode of the test system. The second group tests the accuracy of the system using a signal generator to simulate the operating conditions of an industrial robot and a comparison test using an NI PXIe-4992 acquisition card and the sensors of this system. The third group uses a waveform signal generator to simulate industrial signals and reconstruct waveforms of the acquired data using the software in this paper.

2 Industrial equipment data acquisition system

2.1 ZYNQ Chip

The Zynq-7010 platform utilizes Xilinx's highest-performance K7 family of chips as the core chip for the FPGA portion of the platform. As another part of the Zynq-7010 series platform, the ARM processor has been refined to embed a ZYNQ core and an Ethernet peripheral with gigabit transfer speeds, as well as a network transfer protocol for high-speed and reliable data transfer. As another part of the Zynq-7010 family of platforms, the ARM processor has been refined to embed a ZYNQ core and an Ethernet peripheral with gigabit transfer speeds, and also uses a network transfer protocol for high-speed and reliable data transfer.

The AD7606 has a 16-bit sampling rate with a maximum sampling rate of 200 KSPS. In addition, the input signal interface of the AD7606 is very flexible, and can support a variety of different types of input signals. The AD7606 can complete 4, 6, and 8 channels of synchronous data acquisition. In order to prevent signal overlap and other interfering phenomena in the industrial level data acquisition, it adopts a single power supply operation mode, with on-chip filtering and high resistance. It has on-chip filtering and high-impedance input characteristics. Meanwhile, all its flexible digital filters can be realized through pin driving, which can effectively improve the signal-to-noise ratio and reduce the bandwidth by 3dB. These features make the AD7606 suitable for data acquisition applications that require high signal quality while also providing better flexibility and tunability to meet data acquisition needs in different scenarios.

2.2 System design

In the design of the software program in this paper, the program is divided into five modules, including the analog-to-digital converted data acquisition module, the data output function module, the data writing control module, the data caching module, and the communication interface module.

2.2.1 Industrial equipment data acquisition module

Figure 1 shows the whole process of the whole system acquisition. The AD7606 has 8 channels for data acquisition and includes input protection, signal amplification, filtering, reference, and digital signal processing. The chip is usually used for signal acquisition in industrial equipment, such as power monitoring and protection systems, motor control, instrumentation and control systems, multi-axis positioning, and data acquisition. For 16-channel data acquisition, two AD7606s are used for synchronized data acquisition and display. During data conversion, all channels are synchronized for data acquisition when the BUSY signal is high. After data conversion is finished, the BUSY signal goes low and waits for the subsequent command to be issued during this low state. When CS and RD are both low and in parallel mode, the output bus is activated. Enabling the output bus causes all channels of the AD7606 to be read, and when all channels are read, the data is stored. In order to maintain high precision acquisition of multi-channel count sampling, a symmetrical layout of 2 AD7606 acquisition chips can be used. This layout ensures a good match between the two chips. In order to achieve synchronized sampling. The AD conversion signals CONVSTA and CONVSTB of the two acquisition chips can be connected separately for synchronized control. This layout can make the acquisition system more concise and effectively improve the accuracy and stability of the acquired data. In the design of this system, only one of the eight input channels needs to be used for sampling, so the single-channel sampling mode of the AD7606 can be used. In this mode, it is only necessary to connect the CONVST and ADCCLK signals to the same control signal, and at the same time, in order to realize the synchronous sampling of the system, the use of the master control chip ZYNQ on the two data acquisition chips for unified regulation.

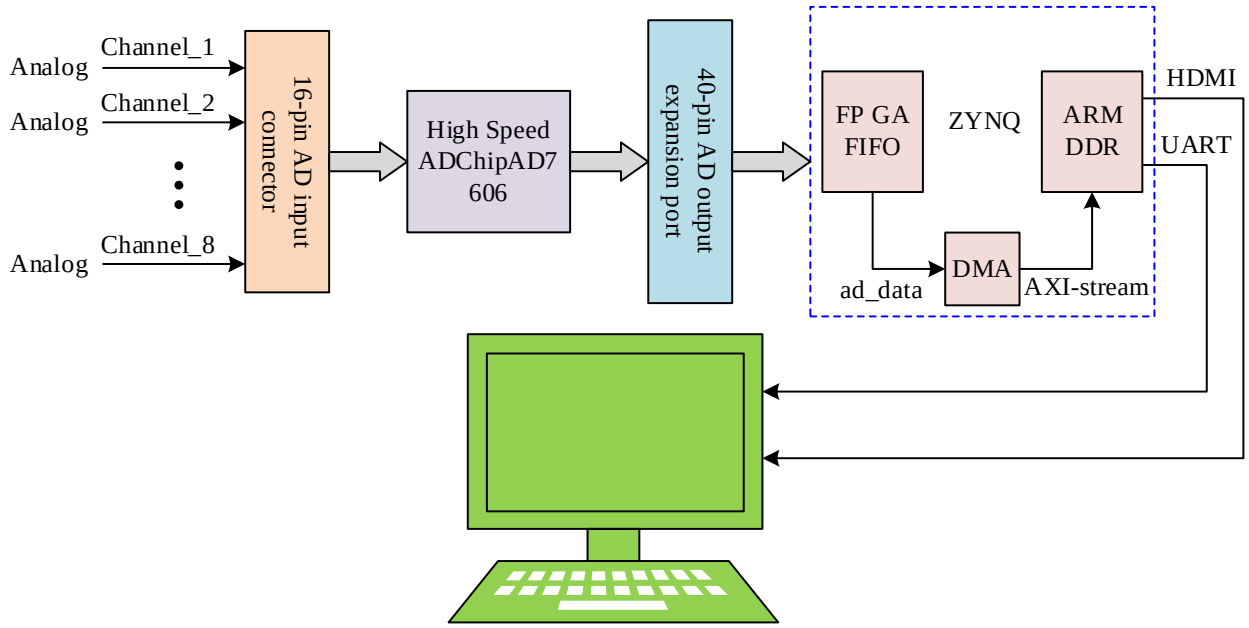


Figure 1. The overall design of the data acquisition system

2.2.2 Signal output function module

According to the system requirements for the design of the waveform data generator, the waveform data generator designed in this system can generate and output sine, square, sawtooth, triangle and self-drawing waveforms, respectively. For the waveform data, the direct output method is chosen, where the waveform generator sends out the signal, then transmits it through the Ethernet, and finally

collects and saves the signal through the system. The other option is to configure the signal parameters according to Ethernet and transmit the data. After the collector completes the above operation, the digital-to-analog converter will read the buffer data and output it directly.

2.2.3 Data Write Control Module and Cache Module

In order to realize the process of storing data after the system has issued commands through the control interface, this system, when carrying out the program design, designs a program for controlling the writing of data in the underlying program of the FPGA, which inputs the data obtained from the data acquisition of this system into the module owned by the software, and controls the operation of the module and the operation of the module, which is carried out to write the obtained data into specific physical addresses in the memory. This operation is performed to write data to specific physical addresses in the memory. At the same time, the program filters out the data from the selected channel and stores it according to the length of the data block. The data writing control program automatically writes the data into memory and sets the data block write full flag when it's full. In this way, data storage and management during data acquisition can be achieved. In the underlying design of the FPGA, the data acquired by the ADC needs to be transferred to the ZYNQ via DMA, and when the transfer is performed, the data acquired by the ADC is not in the same form as the data that the DMA interface can receive, so it is necessary to convert the data acquired by the ADC to the format, that is, to convert the ADC data to the AXIS streaming data format, so that the DMA can easily transfer it. The output data of the ADC is output in the form of parallel data.

In the process of data writing, only the way of writing to the DDR from the outside is selected, and the way of reading data from the DDR is not used. There are two buses and one data interface connected to the control module, which is used for data transmission or the function of module reset, respectively.

2.2.4 PL-PS communication module

Figure 2 shows the information transfer within the chip. In the design of this system, firstly, the clock at the PS side of ZYNQ is set to 100 MHz. Then, the DMA working mode is configured using the address mapping transfer interface, and the data is written to the DDR3 memory. In order to better control the problem of data interaction, the HP high-speed interface is added to the design of the system. Next, the data previously written to the DMA module is subjected to a readout operation, and the readout data is written to the FIFO registers that have already been configured. In this process, 1 interrupt signal is added. Finally, by controlling the DMA and sending the data stream written to the FIFO back to the DDR through the AXI bus, 1 more interrupt signal is added, and the PL side performs 1 read/write operation of the DMA data through the AXI bus to realize the data transfer.

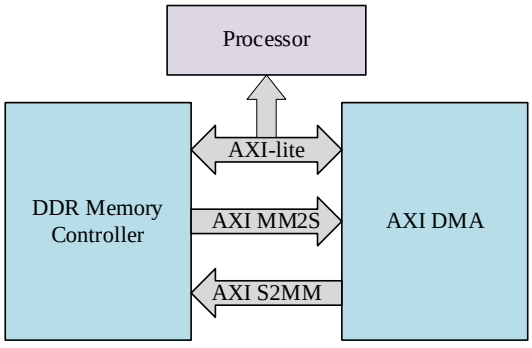


Figure 2. Chip internal data transmission

2.3 Data Acquisition and Fusion

2.3.1 D-S theory of evidence

The basic strategy of the D-S theory of evidence is to divide the collection of evidence into a number of unrelated parts and use each of them to make independent judgments about the identification frames, and then combine them using the rules of combination.

Definition 1 is to make the finite set $\mathrm{U}=\{u_1,u_2\cdots u_n\}$ of all hypotheses under a condition (or evidence) $\mathrm{x}=\{x_1,x_2,\cdots,x_n\}$ an identification frame, and the set consisting of all subsets of U is the power set of U, denoted 2^U.

Definition 2 is a direct support for A given a recognition frame U, a mapping $\mathrm{m}:2^U\to[0,1]$ on its power set 2^U is said $m(A)$ to be the assigned value of the confidence function of A, and $m(A)$ to be the exact degree of confidence in proposition A, when the following conditions are satisfied.

$$m(\phi)=0 \tag{1}$$

$$\sum_{A\subset U} m(A)=1 \tag{2}$$

Definition 3 is such that if $A\subseteq U$, and $m(A)>0$, then A is said to be the focal element.

Definition 4 is to define a function given a recognition box $U,m:2^U\to[0,1]$ is a confidence assignment on U:

$$Bel:2^U\to[0,1] \tag{3}$$

$$Bel(A)=\sum_{B\subset A} m(B)(\forall A\subset U) \tag{4}$$

Call the function Bel a trust function on U, and $Bel(A)=\sum_{B=A} m(B)$ denote the sum of the likelihood measures of all subsets of A, which leads to $Bel(\phi)=0, Bel(U)=1$.

Definition 5, given identification frame U, call $1-Bel(\bar{A})$ the likelihood function of A, denoted $pl(A)$, where $Bel(\bar{A})$ denotes the degree of skepticism about A, i.e., $Bel(\bar{A})$ denotes the degree of certainty that it is not $\bar{A}$, as specified in the following formula:

$$pl(A)=1-Bel(\bar{A}) \tag{5}$$

Then $[Bel(A), pl(A)]$ is said to be the trust interval for A. The trust interval specifies the upper and lower bounds on the level of trust in A.

2.3.2 Combination rules for the D-S theory of evidence

First we provide rules for combining two pieces of evidence. Let m_1 and m_2 be two mutually independent confidence function assignments on 2^U. The question now is how to determine the combined confidence function assignment, $m = m_1 \oplus m_2$.

Theorem 1 Assume that Bel_1 and Bel_2 are two confidence functions on the same identification frame U, and m_1 and m_2 are their corresponding confidence function assignments with focal elements $A_1, A_2, \cdots A_k$ and $B_1, B_2, \cdots B_r$, respectively, and let:

$$K_1 = \sum_{\substack{i,j \\ A_i \cap B_j = \phi}} m_1(A) m_2(B) < 1 \tag{6}$$

Then:

$$\mathrm{m(C)} = \begin{cases} \dfrac{\sum\limits_{\substack{i,j \\ A_i \cap B_j \neq \phi}} m_1(A) m_2(B)}{1 - K_1}, , \forall C \subset U, C \neq \phi \\ 0 \qquad\qquad\qquad , C = \phi \end{cases} \tag{7}$$

In the equation, if $K_1 \neq 1$, then m determines a confidence function assignment. If $K_1 = 1$, then m_1 and m_2 are considered to be contradictory and no combination of confidence function assignments can be made. The rule for combining evidence given by Theorem 1 is called the Dempster combination rule. For the combination of multiple evidences, the Dempster combination rule of Theorem 1 is used to synthesize the evidences two by two. Let the evidence intervals of $A, B \subseteq U, A, B$ be respectively:

$$EI_1(A) = \left[Bel_1(A), pl_1(A) \right] \tag{8}$$

$$EI_2(B) = \left[Bel_2(B), pl_2(B) \right] \tag{9}$$

Then the combined evidence interval is:

$$\begin{aligned} & EI_1(A) \oplus EI_2(B) \\ & = \left[1 - K_2 \left(1 - Bel_1(A) \right) \left(1 - B_e l_2(B) \right), K_2 pl_1(A) pl_2(B) \right] \end{aligned} \tag{10}$$

Among them, $K_2 = \left\{ 1 - \left[Bel_1(A) Bel_2(\bar{B}) Bel_1(\bar{A}) Bel_2(B) \right] \right\}^{-1}$.

The rule of combining two pieces of evidence can be analogized to the rule of combining multiple pieces of evidence.

Theorem 2 Assume that $Bel_1, Bel_2, \cdots, Bel_n$ is the confidence function of n independent evidence on the domain U, and its corresponding confidence assignment functions are $m_1, m_2, \cdots, m_n$.

The corresponding focus elements are $A_{11}, A_{12}, \cdots A_{1k_1}, A_{21}, A_{22}, \cdots A_{2k_2}, \cdots A_{n1}, A_{n2}, \cdots A_{nk_n}$ respectively.

Let $A = A_{1i_1} \cap A_{2i_2} \cap, \cdots A_{ni_n}$

$$K_1 = \sum_{A=\phi} m_1\left(A_{1i_1}\right) m_2\left(A_{2i_2}\right) \cdots m_n\left(A_{ni_n}\right) \tag{11}$$

If $K_1 < 1$, the fused plausibility function is assigned as:

$$m(C) = \frac{\sum_{A \neq \phi} m_1\left(A_{1i_1}\right) m_2\left(A_{2i_2}\right) \cdots m_n\left(A_{ni_n}\right)}{1 - K_1} \tag{12}$$

Usually in the process of multiple evidence fusion, in order to avoid the cumbersome arithmetic caused by the error, generally use the above formula first two evidence fusion results and then fused with the third evidence, and so on, until and the nth evidence fusion to get the final fusion results. For D-S evidence theory, the result is not affected by the order of evidence combination.

Theorem 1 and Theorem 2 give the D-S synthesis rules for two and multiple bodies of evidence, respectively. The reason why the evidence synthesis operation is carried out is to make up for the uncertainty possessed by a single piece of evidence and to improve the reliability of the conclusion of evidential reasoning. However, in practice, can the above goal be achieved after the synthesis of evidence bodies? The exact answer is given below by Theorem 3.

Theorem 3 then sets n the number of bodies of evidence, U the identification frame, satisfies the condition in Theorem 2 that D-S the synthesis rule holds, i.e., the following equation holds, $Bel = Bel_1 \oplus Bel_2 \oplus \cdots \oplus Bel_n$ and then the uncertainty of the synthesized conclusion $m(U)$ is satisfied:

$\exists i \in \{1, 2, \cdots n\}, m_i(U) = 0,$ then $m(U) = 0$.

$\forall i \in \{1, 2, \cdots n\}, m_i(U) \neq 0,$ then $m(U) < m_i(U)$.

Prove the following by mathematical induction:

Let $n = 2$, the following equation holds by the D-S synthesis rule of Theorem 1.

$$m(U) = \frac{\sum_{A_i \cap B_j - U} m_1\left(A_i\right) m_2\left(B_j\right)}{1 - \sum_{A_i \cap B_j - \phi} m_1\left(A_i\right) m_2\left(B_j\right)} \tag{13}$$

$A_i \cap B_j = U$ can be satisfied only if $A_i = U$ and $B_j = U$, so the above equation can be rewritten as:

$$m(U) = \frac{m_1(U) m_2(U)}{1 - \sum_{A_i \cap B_j - \phi} m_1\left(A_i\right) m_2\left(B_j\right)} \tag{14}$$

1) When $m_1(U)=0$ or $m_2(U)=0$, from the above equation, $m(U)=0$.

2) When $m_1(U)\neq 0$ and $m_2(U)\neq 0$, $\sum_{B_j\subseteq U} m\left(B_j\right)=1$.

$\therefore m_2\left(B_j\right)\leq 1-m_2(U)$.

$$\begin{aligned}&\sum_{m_1(A)\cap m_2\left(B_j\right)-\phi} m_1\left(A_i\right)m_2\left(B_j\right)\leq \sum_{m_1\left(A_i\right)\sim m_2\left(B_j\right)-\phi} m_1\left(A_i\right)\left[1-m_2(U)\right]\\&=\left[1-m_2(U)\right]\sum_{m_1\left(A_i\right)\cap m_2\left(B_j\right)-\phi} m_1\left(A_i\right),\end{aligned} \tag{15}$$

And $\sum_{A_i\subseteq U} m\left(A_i\right)=1$.

$\therefore \sum_{m_1\left(A_i\right)\sim m_2\left(B_j\right)-\phi} m_1\left(A_i\right)\leq\left[1-m_1(U)\right]$.

$\therefore \sum_{m_1\left(A_i\right)\sim m_2\left(B_j\right)-\phi} m_1\left(A_i\right)m_2\left(B_j\right)\leq\left[1-m_2(U)\right]\left[1-m_1(U)\right]$.

$\therefore 1-\sum_{m_1\left(A_i\right)\cap m_2\left(B_j\right)-\phi} m_1\left(A_i\right)m_2\left(B_j\right)\geq m_2(U)+m_1(U)-m_2(U)m_1(U)$

May as well set up:

$$m_1(U)\leq m_2(U) \tag{16}$$

Then by Eq. This can be seen:

$$\begin{aligned}&m(U)<\frac{m_1(U)m_2(U)}{\left(m_1(U)+m_2(U)-m_1(U)m_2(U)\right)}=\\&\frac{m_1(U)}{1+\frac{m_1(U)}{m_2(U)}-m_1(U)}=\frac{m_1(U)}{1+m_1(U)\frac{1-m_2(U)}{m_2(U)}}\leq m_1(U)\end{aligned} \tag{17}$$

From the above equation, $m(U)<m_2(U)<m_1(U)$. Hence, Theorem 3 holds when $n=2$.

Set $n=k$ when the uncertainty of the synthesis of these k evidences is $m^{(k)}(U)$, when Theorem 3 holds for $\exists i\in\{1,2,\cdots,k\}, m_i(U)=0$, then $m^{(k)}(U)=0\forall i\in\{1,2,\cdots,k\}, m_i(\Theta)\neq 0$, then $m^{(k)}(U)<m_i(U)$.

It is proved below that when $n=k+1$, the synthesized uncertainty $m^{(k+1)}(U)$ satisfies Theorem 3.

At this point it is equivalent to the two evidences $m^{(k)}$ and m_{k+1} to perform the synthesis operation, and from step (1), the following relation exists:

$$m^{(k+1)}(U)=\frac{m^{(k)}(U)m_{k+1}(U)}{1-\sum_{\mathrm{A_i}\cap B_j-\phi} m^{(k)}\left(\mathrm{A_i}\right)m_{k+1}\left(B_j\right)} \tag{18}$$

From the above equation:

1) When $\exists i\in\{1,2,\cdots,k\}, m_i(U)=0, m_i(U)=0$, then $m^{(k)}(U)=0$. so $m^{(k+1)}(U)=0$.

When $m_{k+1}(U)=0$, then $m^{(k+1)}(U)=0$. In short, $\exists i\in\{1,2,\cdots,k,k+1\}, m_i(U)=0$, then $m^{(k+1)}(U)=0$.

2) When $\forall i\in\{1,2,\cdots k+1\}, m_i(U)\neq 0$, the same reasoning process as in step (1) can also be proved $m^{(k+1)}(U)<m^{(k)}(U)$ and $m^{(k+1)}(U)<m_{k+1}(U)$ and because $\forall i\in\{1,2,\cdots k\}$, $m_i(U)\neq 0$, then $m^{(k)}(U)<m_i(U)$. So, can be obtained:

$$\forall i\in\{1,2,\cdots,k,k+1\}, m_i(U)\neq 0, \text{then } m^{(k+1)}(U)<m_i(U) \tag{19}$$

In summary, Theorem 3 holds.

Thus, from Theorem 3, it follows that as more evidence is involved in the synthesis operation, the uncertainty of the synthesized evidence becomes smaller and smaller, and the reliability of the inference conclusions becomes higher.

3 Industrial equipment acquisition system application and test

3.1 Performance testing

Before testing the system solution designed in this paper, it is first necessary to measure the overall power consumption of the system in normal operating mode, idle mode and sleep mode. In the test, a DC energy meter is connected to the 24V input port of the overall power supply of the system, which can display the total real-time input current of the system. In the normal operating mode, the operating frequency of the system can be adjusted. The highest adjustable operating frequency is 555MHz, and the lowest operating frequency is 111MHz. The system power consumption test process is to make the system in the normal operating mode of the high-frequency state, the low-frequency state of the normal operating mode, the idle mode and the hibernation mode switching, each time after switching the state after the state is stabilized for 30 seconds, the total system current value of the state is read. The total current value of the system in this state is read after the state stabilizes for 30 seconds after each switching state. The 10 sets of data for the system power consumption test are shown in Figure 3.

The highest system consumption is 261mA, and the lowest is 255mA under high-frequency output, with a difference of 6mA. The device output is normal under high frequency. The lowest consumption in the low-frequency condition is 229mA and the highest is 234mA, with a difference of 5mA, and the system maintains normal in the low-frequency condition. In the case of idle mode, the peak

difference is 7mA. Leisure mode and high-frequency state are consistent. The difference between the highest and lowest is 6mA, which is more stable.

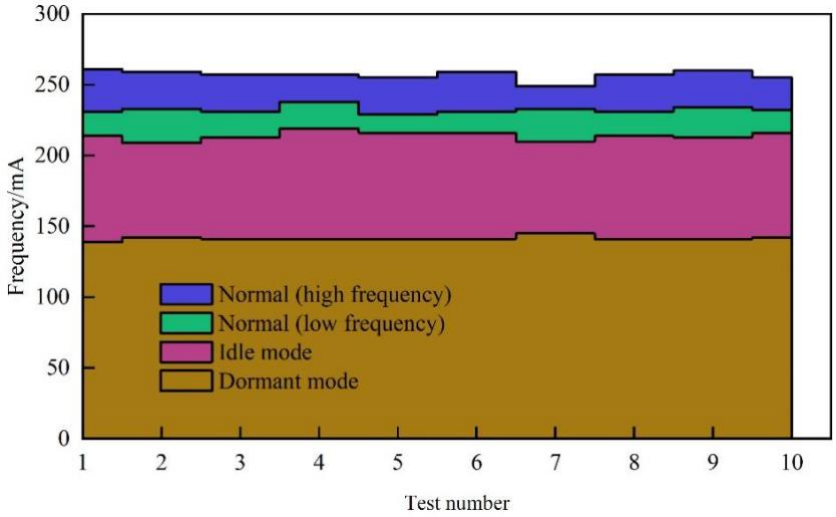


Figure 3. System current condition

The two timeout thresholds for the dynamic multi-mode management strategy during testing were set to 100 ms and 10 s. The intensity of the test tasks was categorized into two types: one with a random number of tasks at intervals between 0 and 30 seconds and the second with a random number of tasks at intervals between 0 and 50 seconds. The test tasks were performed at random intervals between 0 and 30 s. The test tasks were performed at random intervals between 0 and 50 s. The process of each test experiment is 30 minutes, and the overall current value of the system is read every 3-minute interval during the test. Table 1 shows the results of this system test. As can be seen from the test results, the system is very stable, with a negligible difference of 1.7mA in the average value of the current while executing the two task sets. The difference in power consumption is equally small. In the execution of PM1~PM3, the difference is 0.82%, 3.35%, and 6.27%, respectively, and the gap range is not more than 10%. It can be seen that the system designed in this paper is stable in operation.

Table 1. Current mean

	Noramal	PM1	PM2	PM3
Test task set 1	263.2	244.6	195.1	186.2
Power consumption		6.54%	25.41%	27.89%
Test task set 2	261.5	237.0	179	171.5
Power consumption		7.36%	28.76%	34.16%

3.2 Data Acquisition Accuracy Tests for Industrial Equipment

3.2.1 Industrial Robot Signal Acquisition Testing

A signal amplifier was used to vibrate the drive table to mimic the operating state of an industrial robot, followed by sensor data acquisition using the system in this paper to test the software in this paper. The NI PXIe-4992 acquisition card is used, and the chassis is PXIe-1071. The signal generator produces a 1kHz sinusoidal signal, which is amplified by a power amplifier to drive the vibration table, which vibrates at the same frequency as the signal generator. The shaker is a Modal Shop 2075E, and the power amplifier is a SmartAmp-2100E21 with a magnification of 2.0. Two IEPE acceleration

sensors are placed in symmetrical positions on the shaker, and the sensor is a PCB 352C03. The sampling rate of the monitoring system and the NI acquisition is set to 125kHz, the gain is set to 1x, and the IEPE excitation is turned on with AC coupling. Coupling, and turn on the IEPE excitation source. After the monitoring system and NI acquisition card are collectively acquired for a period of time, the upper computer reads the data for comparison, and the results are shown in Figure 4. FFT analysis of the measured data frequency shows that the peak frequency is 1000.000Hz, consistent with the input signal.

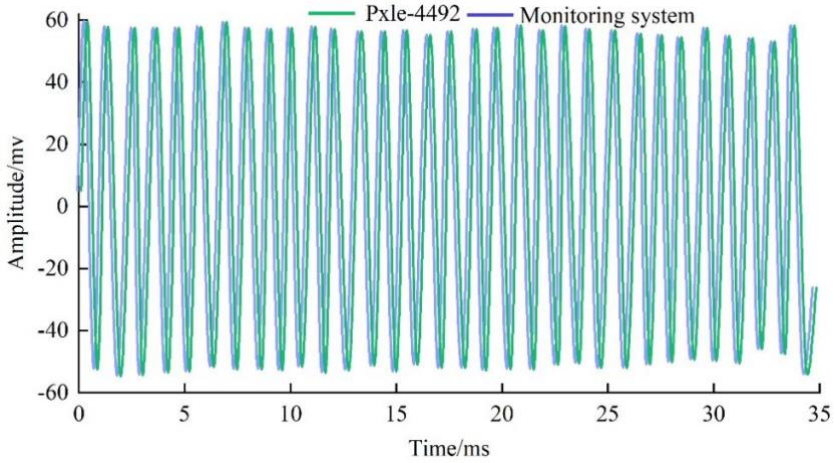


Figure 4. Accuracy test

This paper's hardware acquired signal peak value of 94.18mv, and NI acquisition card signal peak value of 97.26mv. The error between the two is only 3.08. This is due to the sensor placement not being completely symmetrical and the two completely at the same time acquisition. The test results show that the hardware of this paper and the NI acquisition card measurement results are very similar, which verifies that the acquisition system of this paper can accurately collect the IEPE sensor signals.

3.2.2 Industrial equipment signal acquisition testing

An arbitrary waveform signal generator is used to output a sine wave and feed it into the data acquisition board to mimic industrial equipment signals for on-line testing of the system. First, the data is streamed through the AXI4-Stream bus and then stored in the DDR through the HP interface. Waiting for the completion of the data transfer, the data in the memory is taken out, and the waveform is reconstructed. The spectrum is analyzed by MATLAB software on the PC. The main tools used for the system performance test are a signal generator, IF digital demodulation system and MATLAB software. The signal generator is RIGOL DG1022U.

The performance characteristics can be divided into two categories: static characteristics and dynamic characteristics and this topic mainly tests the dynamic characteristics, including the spurious-free dynamic range, the effective number of bits, etc. There are two categories of dynamic characteristics of the signal generator: static characteristics and dynamic characteristics. The sine wave fitting method and frequency domain analysis method are the primary test methods used to assess dynamic characteristics. Compared with the sine wave fitting method, the frequency domain analysis method does not introduce source noise in the testing process, which can better suppress the additional interference, and at the same time, more index parameters can be tested, so this method is used to test the dynamic performance. The signal generator generates a 1MHz sine wave, connects the signal transmitting port to the data acquisition board through the SMA transmission line, and imports the sampled data into the MATLAB software for waveform reconstruction and spectral analysis, and the

time-domain and spectral waveforms are shown in Figure 5. The acquisition situation is stable. There is no interruption phenomenon; the data collected by the acquisition equipment reaches a peak value of 2.0, and the trough is basically the same, between -1.5 and -1.8. The final calculation yields a signal-to-noise ratio of 50.12 dB for the sampled signal, and the effective number of bits reaches 10.40 bits.

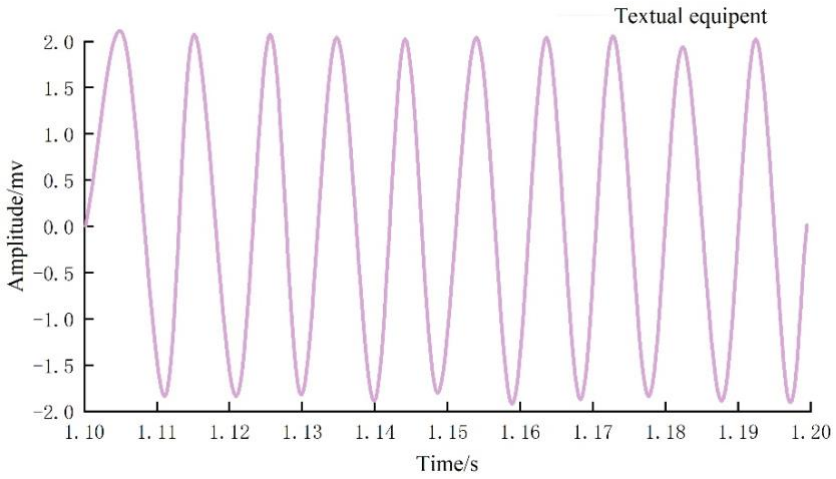


Figure 5. Rebuild wave mode time domain

Figure 6 shows the frequency domain of the reconstructed waveform, and it can be seen that the device has a peak between frequency 0-2, and the amplitude reaches 22. But it quickly declines and stabilizes between 0-5, and there is no more big fluctuation. This experiment can prove that the dynamic performance indicators of the system are in line with the typical values of the dynamic parameters of the device, the acquisition module works well, and the display module waveforms are free of distortion.

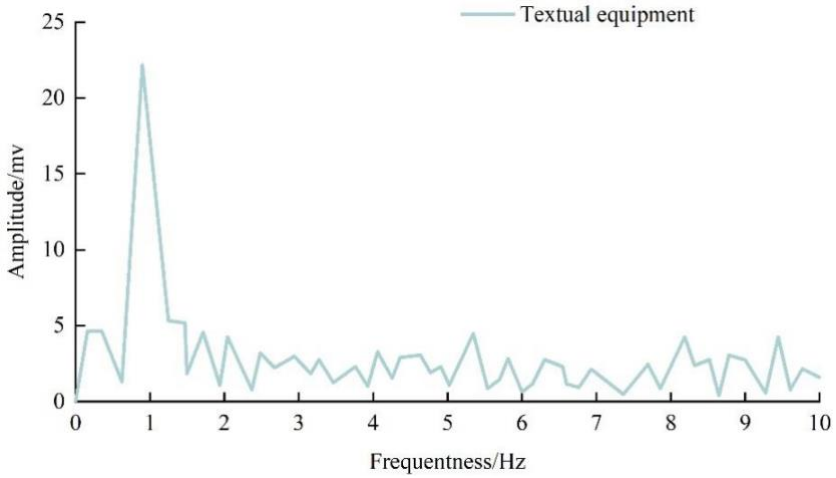


Figure 6. Restructure of the wave frequency domain

4 Conclusion

In this paper, ZYNQ is used as the hardware basis to design the industrial equipment data acquisition system, applying the data fusion technology based on the D-S evidence theory of typical samples to the data acquisition, fault diagnosis of the equipment, and proving its validity and practicability by

taking the simulation experiments of the actual data and achieving the intended effect. As follows are the conclusions of this paper:

1) The system has relatively high stability. The difference in the average value of current when the system is performing the test task set is 1.7mA, which is almost negligible. The difference in power consumption is not more than 10%, and in the output modes of high frequency and low frequency, the difference in the respective mode current cases is also not more than 10 mA. There is no breakpoint in the execution of the test.

2) The accuracy of the industrial equipment acquisition system can be improved by using a combination of typical samples and D-S evidence theory, determining the confidence function allocation, and performing data fusion of individual data for data acquisition processing. In the accuracy test, the monitoring system and the NI acquisition sampling rate are set to 125 kHz, the gain is set to 1x, and after a period of time, the measured data frequency is analyzed by FFT, and the results show that the frequency peaks are all 1000.000 Hz, which is consistent with the input signal. The waveforms were stabilized between -60 and 60 without interruption.

3) Good acquisition of industrial equipment. The use of arbitrary waveform signal generator output sine wave and sent to the data acquisition board using the system to reconstruct the waveform, the acquisition situation is stable, there is no interruption phenomenon, the collection of data collected by the device peak reached 2.0, the trough is basically the same, between -1.5 and -1.8. The final calculation yields a signal-to-noise ratio of 50.12 dB for the sampled signal, with an effective bit count of 10.40 bits. The system shows a peak between frequency 0-2 with an amplitude of 22. However, it quickly drops and stabilizes between 0-5 without further major fluctuations.

References

[1] Lin, J., Liao, J., Zhang, Z., Lin, H., & Zhang, J. W. (2021). Design of data acquisition system in tobacco industry based on industrial internet of things. Journal of Physics: Conference Series, 1965(1), 012034-.

[2] Lesjak, C., Ruprechter, T., Bock, H., Haid, J., & Brenner, E. (2014). Facilitating a secured status data acquisition from industrial equipment via nfc. International Journal of Internet Technology and Secured Transactions, 3(3), 288-299.

[3] Cui, Y. (2022). Study on abnormal data acquisition method of industrial internet of things communication based on node clustering. International journal of data mining and bioinformatics.

[4] Promsuk, N., & Taparugssanagorn, A. (2021). Numerical reader system for digital measurement instruments embedded industrial internet of things. J. Commun., 16, 132-142.

[5] Maseda, F. J., Iker López, Martija, I., Alkorta, P., Garrido, A. J., & Garrido, I. (2021). Sensors data analysis in supervisory control and data acquisition (scada) systems to foresee failures with an undetermined origin. Sensors(8).

[6] Liu, D., Zhen, H., Kong, D., Chen, X., Zhang, L., & Yuan, M., et al. (2021). Sensors anomaly detection of industrial internet of things based on isolated forest algorithm and data compression. Scientific Programming.

[7] Haleem, S. L. A., Kshirsagar, P., Manoharan, H., Prathap, B., H., S., & Kumar, K. P., et al. (2022). Wireless sensor data acquisition and control monitoring model for internet of things applications. Scientific Programming.

[8] Ok, J. S., Kwon, S. D., Heo, C. E., & Suh, Y. K. (2021). A survey of industrial internet of things platforms for establishing centralized data-acquisition middleware: categorization, experiment, and challenges. Hindawi Limited.

[9] Jang, Y. M. (2022). Real-time energy data acquisition, anomaly detection, and monitoring system: implementation of a secured, robust, and integrated global iiot infrastructure with edge and cloud ai. Sensors, 22.

[10] Manogaran, G., Alazab, M., Shakeel, P. M., & Hsu, C. H. (2021). Blockchain assisted secure data sharing model for internet of things based smart industries. IEEE Transactions on Reliability, PP(99), 1-11.

[11] Izagirre, U., Andonegui, I., Landa-Torres, I., & Zurutuza, U. (2022). A practical and synchronized data acquisition network architecture for industrial robot predictive maintenance in manufacturing assembly lines. Robotics and Computer-Integrated Manufacturing, 74, 102287-.

[12] Lee, J., Lee, Y. C., & Kim, J. T. (2021). Migration from the traditional to the smart factory in the die-casting industry: novel process data acquisition and fault detection based on artificial neural network. Journal of Materials Processing Technology, 290, 116972.

[13] Li, X., Yin, Z., Xu, F., Zhang, F., & Xu, G. (2021). Design and implementation of neural network computing framework on zynq soc embedded platform. Procedia Computer Science, 183, 512-518.

[14] Ballinger, N. (2021). Data acquisition with pacs and plcs. Electronics World(TN.2007), 127.

[15] Zhu, K., Joshi, S., Wang, Q. G., & Hsi, J. F. Y. (2019). Guest editorial special section on big data analytics in intelligent manufacturing. IEEE Transactions on Industrial Informatics, 15(4), 2382-2385.

[16] Cetinceviz, Y., Uygun, D., & Gungor, Y. (2020). An effective speed controller and gprs based data acquisition system design for dc motors. Review of Scientific Instruments, 91(3), 035120.

[17] Li, T., Jingxiang, L., & Xiaoguang, Z. (2018). Design of power data acquisition system based on lpwan.

[18] Okafor, K. C., & Obayi, A. A. (2020). Industry 4.0 cami: an elastic cloud zynq ultrascale fpga metering architecture. Lecture Notes in Computer Science, 12254, 527-543.

[19] Kvasnicka, J., & Collaboration, F. (2017). Data acquisition system for the calice ahcal calorimeter. Journal of Instrumentation, 12(3).

[20] A, A. R., B, R. T., & C, A. A. P. (2020). Parameter extraction of psp mosfet model in multi-core zynq soc platform. Procedia Computer Science, 171, 1027-1036.