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Implementation Possibilities of SMD Capacitors for High Power Applications

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***Abstract* – Focus is on implementation possibilities of surface-mount device (SMD) to be used in high power applications. SMD capacitors reduce the size and dimensions of a power circuit and increase the flexibility of placement of other components. Ceramic and electrolytic capacitors are compared by means of voltage ripple, volume, labour-intensity and impedance. A 1 kW experimental setup of a quasi-Z-Source inverter (qZSI) based converter was built to compare SMD capacitor performance in the quasi-Z-source (qZS) network.**

***Keywords* – Power conditioning, switched-mode power supply, power capacitors, surface-mount technology.**

I. Introduction

Capacitors are one of the basic passive elements in different electric circuits. Today's types of capacitors offered in the market are varied, optimized for different kinds of applications. Also, the range of choices for capacity and operation voltage is very wide.

The field of power electronics cannot be imagined without capacitors that limit the growth of voltage (voltage ripple). Operation voltage is always the limiting factor for a capacitor and accordingly for the dimensions of the whole system. Usually for the same size of a capacitor, the smaller the capacity, the higher is the operation voltage of a capacitor. Since this fact is significant, for it affects the power density and dimensions of the whole system [1, 2], it was decided to use SMD capacitors in the power circuit.

The aim of this paper is to implement and compare different types of SMD capacitors available in the market for a 1 kW quasi-Z-source inverter (qZSI) based step-up converter (Fig.1.) [3, 4]. To provide 1.4 % voltage ripple on a DC-link the capacitance of capacitors should be 220 µF. Since the rated voltage of the DC-link is 80 V, capacitors of at least 100 V should be selected.

II Idea of Experiment

A. Experimental Setup

The circuit diagram in Fig. 1 consists of a VSI coupled with a qZS-network (C_1, C_2, L_1, L_2, D). Based on the input voltage, the operating modes of the proposed DC/DC converter could be broadly categorized as non-shoot-through and shoot-through operating modes [3, 4]. If the input voltage is equal or higher than the desired DC-link voltage, the converter works in the non-shoot-through mode. In this mode, the qZSI operates as a traditional VSI, performing only the buck function of the input voltage.

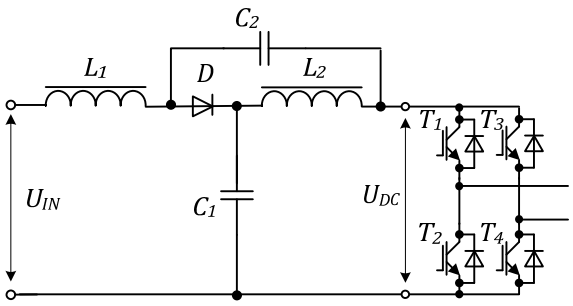


Fig. 1. General circuit diagram used in the experiments.

The operating period of the qZSI in the non-shoot-through operating mode consists of the combination of active and zero states, explained in detail in [4].

If the input voltage drops below the predefined DC-link voltage level, the converter starts to operate in the shoot-through mode. During the shoot-through states the upper and lower switches of one or both phase legs are conducting (i.e., both devices are conducting) [3, 4].

In general, each operating period of the qZSI during the shoot-through mode always consists of an active state t_A, a shoot-through state t_S and a zero state t_Z:

$$T = t_A + t_S + t_Z , \tag{1}$$

$$\frac{t_A}{T} + \frac{t_S}{T} + \frac{t_Z}{T} = D_A + D_S + D_Z = 1 , \tag{2}$$

where D_A is the duty cycle of an active state, D_S is the duty cycle of a shoot-through state and D_Z is the duty cycle of a zero state.

Table I shows general operation and component ratings.

TABLE I
General Operation and Component Ratings

Parameter	Value
Minimal input voltage, $U_{IN(min)}$	40 V
Nominal input voltage, $U_{IN\ (nom)}$	80 V
Desired DC-link voltage, U_{DC}	80 V
System power rating, P	1000 W
Operation frequency of a qZS-network, f_{qZS}	60000 Hz
Desired voltage ripple across the DC-link	1.4 %
Inductance of inductors L_1, L_2	50µH

B. Capacitor Parameter Calculations

At the steady state the average voltage of the capacitors can be calculated as follows:

$$U_{C1} = \frac{1 - D_S}{1 - 2 \cdot D_S} \cdot U_{IN} \quad (3)$$

and

$$U_{C2} = \frac{D_S}{1 - 2 \cdot D_S} \cdot U_{IN} . \quad (4)$$

The DC-link voltage across the inverter bridge is the sum of both capacitor voltages, expressed as

$$u_{DC} = U_{C1} + U_{C2} = \frac{1}{1 - 2 \cdot D_S} \cdot U_{IN} . \quad (5)$$

During the active state, both of the capacitors are connected in series and limit the voltage ripple on the DC-link [4]. It is assumed that the capacitances of the capacitors are equal and can be calculated as

$$C = \frac{2 \cdot P \cdot D_S}{U_{IN} \cdot U_{DC} \cdot f \cdot r_{V,DC}} = \\ = \frac{2 \cdot 1000 \cdot 0.25}{40 \cdot 80 \cdot 50000 \cdot 0.014} \approx 220 \mu F , \quad (6)$$

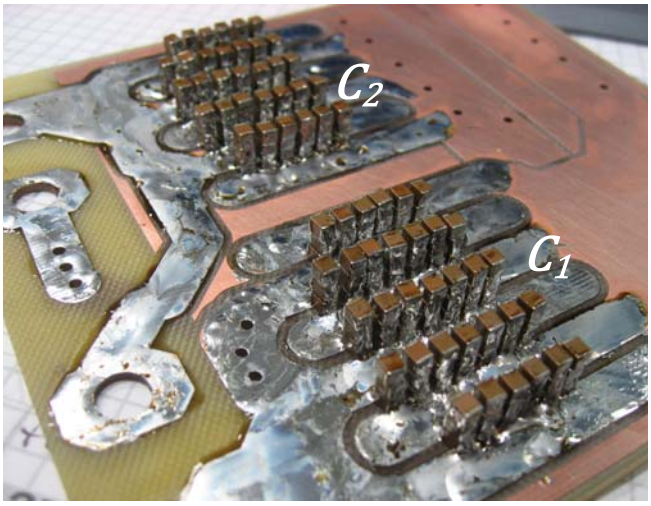
where P is the power rating of the converter, U_{IN} is the input voltage, U_{DC} is the DC-link voltage, D_S is the duty cycle of shoot-through states, f is the operation frequency of the qZSI, and $r_{V,DC}$ is the desired peak to peak voltage ripple across the DC-link.

C. Capacitors Selected for Experiments

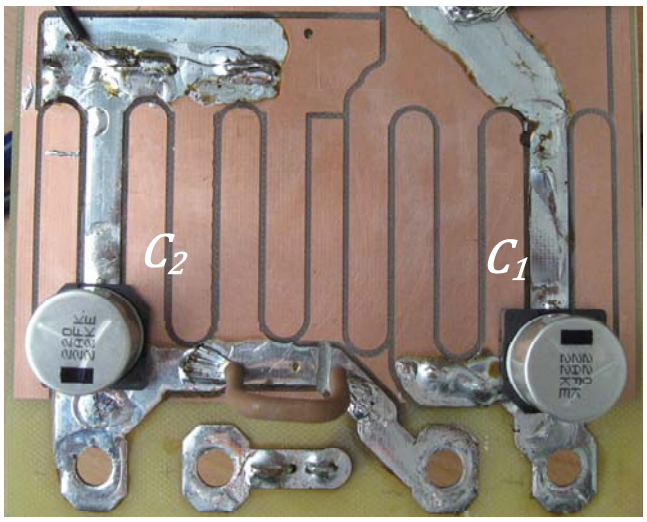
According to operation voltage range (100 V) ceramic capacitor "Murata" (GRM32ER72A225K) [5] with a capacitance of 2.2 µF and Aluminum electrolytic capacitor from "Panasonic" (EEEFK2A221AM) [6] with a capacitance of 220 µF were selected for further study. Since the capacitance of a ceramic capacitor is 2.2 µF, they were soldered 100 in parallel to obtain 220 µF.

For experimental verification, two similar qZS-networks were built - with electrolytic capacitors and with ceramic capacitors. Fig. 2*a* presents a PCB where 200 SMD capacitors are soldered to obtain the capacitance of 220 µF per each qZSI capacitor (C_1 and C_2). Each capacitor (C_1 and C_2) consists of 100 SMD capacitors that are arranged in 33 columns. There are 3 SMD capacitors in one column. Such arrangement was selected in order to make more compact design. Fig. 2*b* presents a PCB where two 220 µF electrolytic capacitors (C_1 and C_2) are used.

Foil capacitors were not selected because of their too small capacitance of 100 V and too high costs compared with electrolytic and ceramic capacitors (Fig. 3).



(a)



(b)

Fig. 2. Capacitances C_1 and C_2 that consist of 200 SMD capacitors (a) and electrolytic capacitors (b).

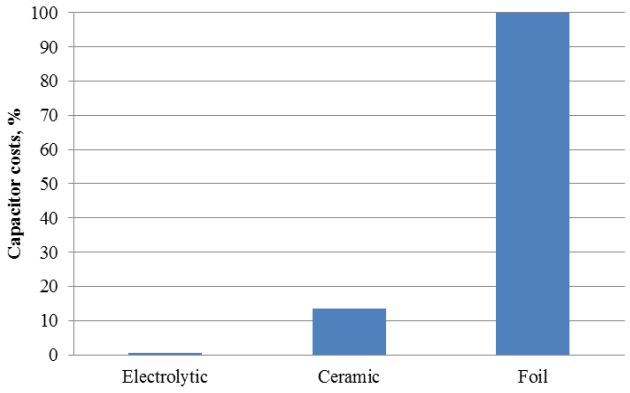


Fig. 3. Capacitor price comparison.

III. Analysis of Experimental Results

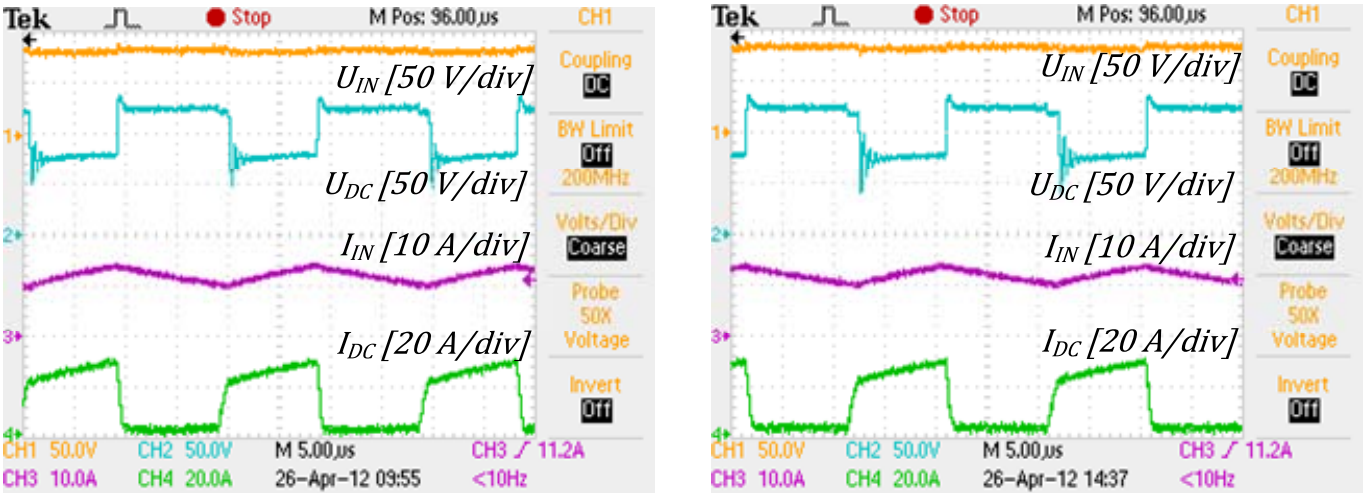
A. General Operation Waveforms

The experimental verification of both capacitor types were carried out at different operation points, i.e. the input voltage was changed from $U_{IN,(min)}$ (40V) up to $U_{IN,(nom)}$ (80V) and D_S was regulated so that the DC-link voltage remained at 80 V.

Fig. 4 shows the input voltage (U_{IN}), the DC-link voltage (U_{DC}), the input current (I_{IN}) and the DC-link current (I_{DC}) of the converter operating with electrolytic (Fig. 4*a*) and ceramic (Fig. 4*b*) capacitors when the input voltage is at its rated value (80 V).

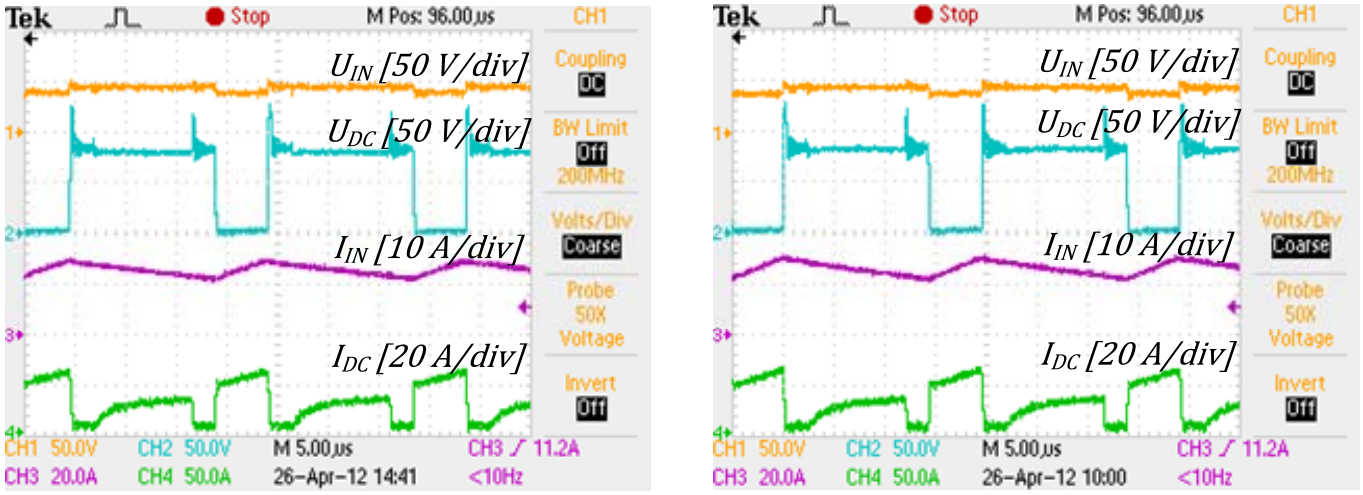
Fig. 5 presents the input voltage (U_{IN}), the DC-link voltage (U_{DC}), the input current (I_{IN}) and the DC-link current (I_{DC}) of the converter operating with electrolytic (Fig. 5*a*) and ceramic (Fig. 5*b*) capacitors when the input voltage is at its minimal value (40 V).

Fig. 6 shows the capacitor C_1 voltage (U_{C1}), the capacitor C_2 voltage (U_{C2}), the capacitor C_1 current (I_{C1}) and the capacitor C_2 current (I_{C2}) of the converter operating with electrolytic (Fig. 6*a*) and ceramic (Fig. 6*b*) capacitors when the input voltage is at its nominal value (80 V).



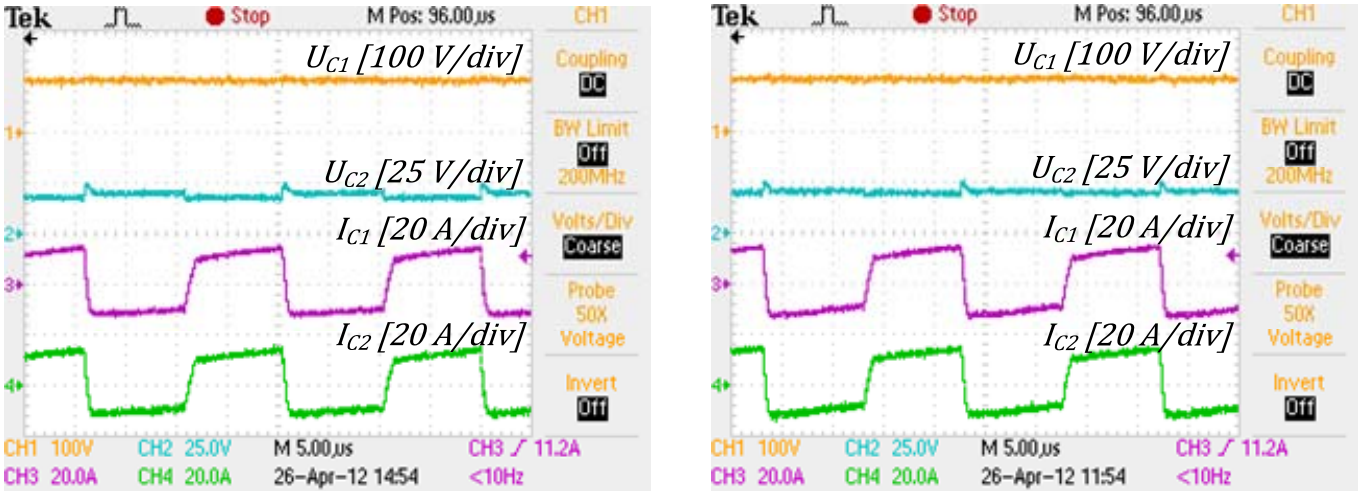
(a) (b)

Fig. 4. Operation waveforms (U_{IN}, U_{DC}, I_{IN}, I_{DC}) of a qZSI with electrolytic capacitors (a) and with ceramic capacitors (b) at U_{IN}=80 V.



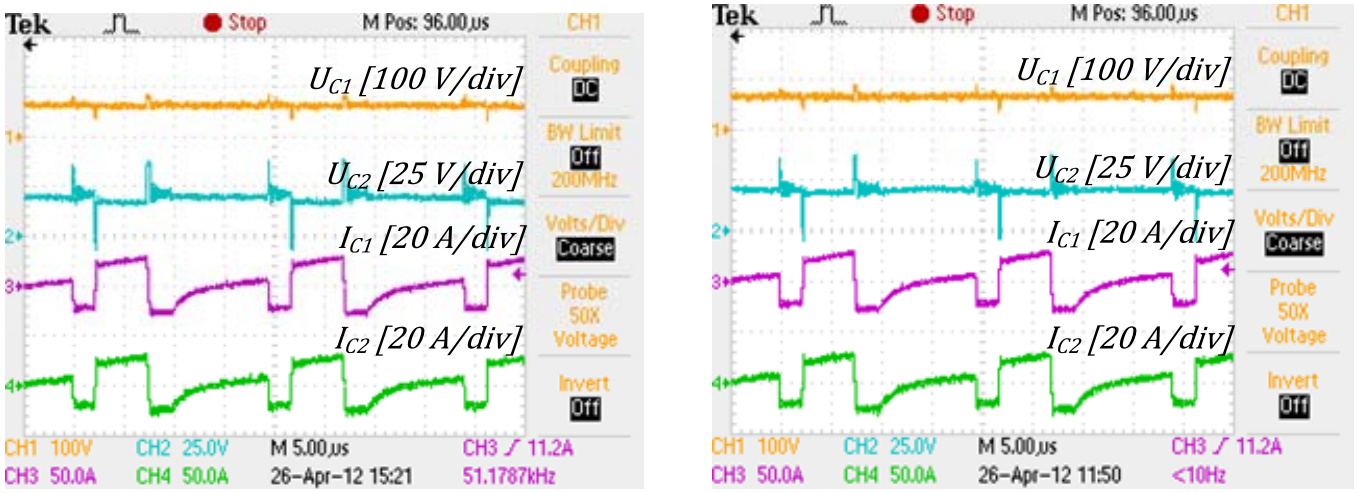
(a) (b)

Fig. 5. Operation waveforms (U_{IN}, U_{DC}, I_{IN}, I_{DC}) of a qZSI with electrolytic capacitors (a) and with ceramic capacitors (b) at U_{IN}=40 V.



(a) (b)

Fig. 6. Operation waveforms (U_{C1}, U_{C2}, I_{C1}, I_{C2}) of a qZSI with electrolytic capacitors (a) and with ceramic capacitors (b) at U_{IN}=80 V.



(a) (b)

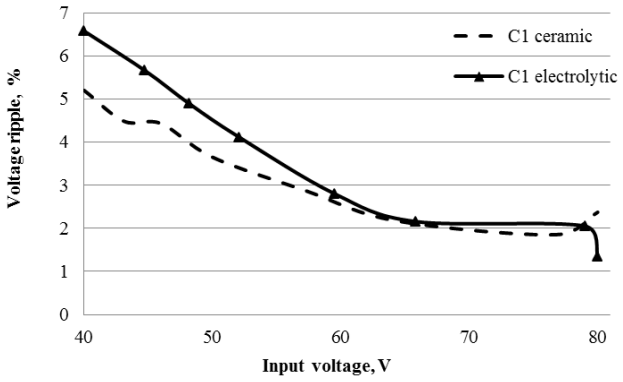
Fig. 7. Operation waveforms (U_{C1}, U_{C2}, I_{C1}, I_{C2}) of a qZSI with electrolytic capacitors (a) and with ceramic capacitors (b) at U_{IN}=40 V.

Fig. 7 presents the capacitor C_1 voltage (U_{C1}), the capacitor C_2 voltage (U_{C2}), the capacitor C_1 current (I_{C1}) and the capacitor C_2 current (I_{C2}) of the converter operating with electrolytic (Fig. 7*a*) and ceramic (Fig. 7*b*) capacitors when the input voltage is at its minimal value (40 V).

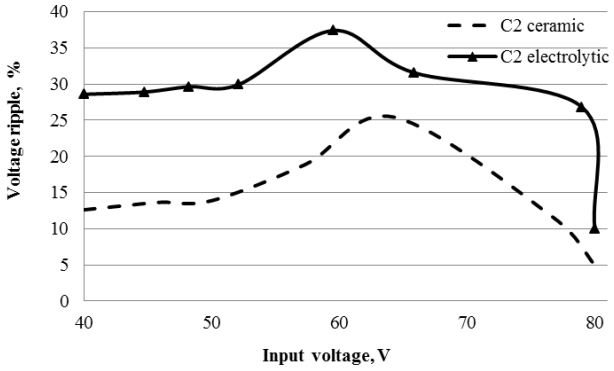
B. Voltage Ripple

To prove capacitor performance in voltage ripple damping the capacitor voltage ripple of both qZSI capacitors (C_1 and C_2) were examined separately.

Fig. 8 presents the voltage ripple of an electrolytic and a ceramic capacitor. It can be seen that the difference between the capacitor C_1 voltage ripple is greater in input voltage range from 40 V up to 60 V (Fig. 8*a*). In the input voltage range from 60 V up to 80 V the difference is negligible. Fig. 8*b* shows that big difference in capacitor C_2 voltage ripple is in whole range of input voltage (from 40 V up to 80 V).



(a)



(b)

Fig. 8. Comparison of voltage ripple using ceramic and electrolytic capacitors: capacitor C_1 (a) and capacitor C_2 (b).

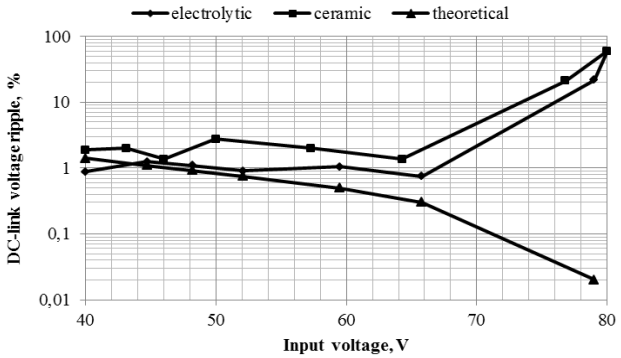
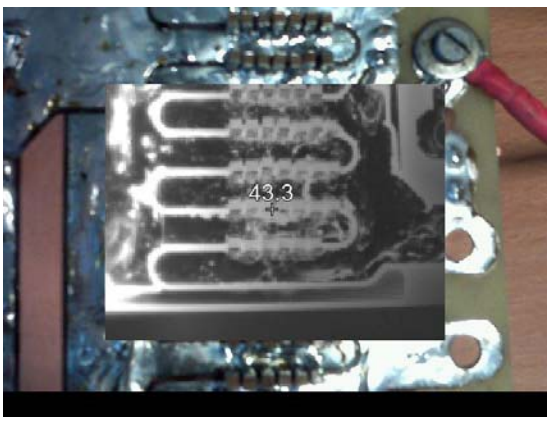


Fig. 9. Dependence of capacitor voltage ripple on the input voltage.

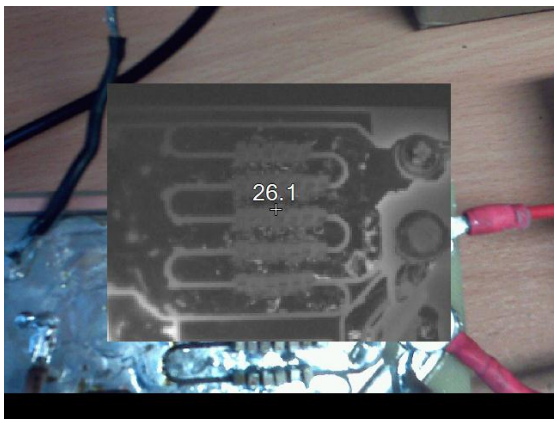
Fig. 9 presents experimental and theoretical voltage ripple on the DC-link during the active state when capacitors (C_1 and C_2) are in series. In the input voltage range up to 65 V, the voltage ripple in both capacitor types is close to the theoretical curve. In the input voltage range from 65 V up to 80 V, the measured and theoretical voltage ripples are not in agreement. These phenomena can be explained by the over-boost effect. It means that the qZS-network itself can cause an increase in the DC-link voltage.

IV. Comparison of Power Losses

Usually power losses can be associated with heat emission. Temperature measurements with thermal imager for both capacitor types were made after 2 minutes working. Fig. 10*a* presents the case of minimal input voltage (U_{IN}=40 V) and maximal shoot-through duty-cycle in order to obtain nominal voltage on the DC-link (U_{DC}=80 V). Fig. 10*b* shows the case of maximal input voltage (U_{IN}=80 V) and minimal shoot-through duty-cycle.

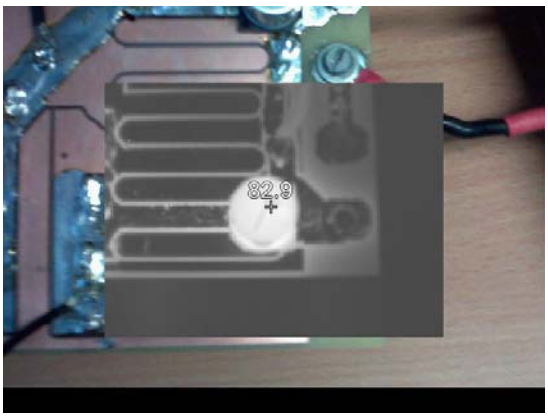


(a)

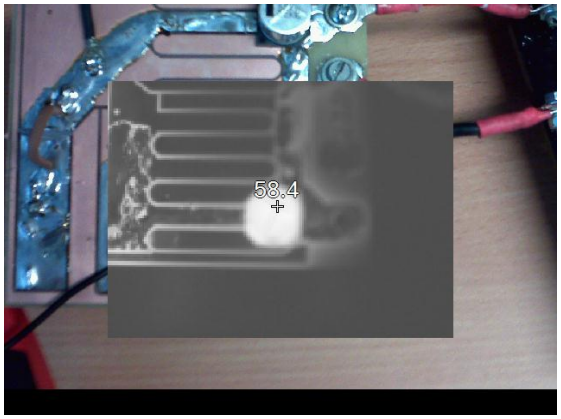


(b)

Fig. 10. Temperature measurement of ceramic capacitors: at minimal input voltage (40 V) (a) and at maximal input voltage (80 V) (b).



(a)



(b)

Fig. 11. Temperature measurement of electrolytic capacitors: at minimal input voltage (40 V) (a) and at maximal input voltage (80 V) (b).

Fig. 11 shows the same measurement technique that was used for electrolytic capacitors.

It can be seen that the surface temperature of electrolytic capacitors (Fig. 11) is around two times higher than that of ceramic capacitors (Fig. 10) in both operation extremes (at minimal and nominal input voltage).

It can be explained by the facts from capacitor data sheets that the ESR of an electrolytic capacitor is given 0.75 Ω (at 120 Hz) but the ESR of one ceramic capacitor is around 3 Ω (at 120 Hz). But since the ceramic capacitor actually consists of 100 SMD ceramic capacitors soldered in parallel, actually 3 Ω should be divided on 100, thereby we obtain 0.03 Ω.

Generally, active power losses in capacitor can be expressed as

$$P_{loss} = I_{C(RMS)}^2 \cdot ESR\,, \tag{7}$$

where $I_{C(RMS)}$ is the RMS value of the capacitor current and ESR is equivalent series resistance.

In some cases there is given dissipation factor or loss tangent (tanδ) and then power losses in capacitor can be expressed as

$$P_{loss} = \frac{\tan\delta}{2 \cdot \pi \cdot f \cdot C} \cdot I_{C(RMS)}^2 \cdot \tag{8}$$

Temperature rise of capacitor can be expressed as

$$\Delta T = (T_s - T_a) = I_{C(RMS)}^2 \cdot ESR \cdot R_{th}\,, \tag{10}$$

where T_s is surface temperature, T_a is ambient temperature and R_{th} (°C/W) is thermal resistance.

Usually ESR as well as impedance depending on the frequency are given in the capacitor data sheets.

Also very important fact that should be taken into account is ripple current. The data sheet of electrolytic capacitor says that ripple current at 100 kHz should not exceed 0.9 A. Our experiments show that ripple current significantly exceed recommended. To check how this fact affect temperature raises it was decided to solder 2 additional capacitors in parallel with existing C_1 and 2 additional capacitors in parallel with existing C_2. The experiments showed that temperature of electrolytic capacitors didn`t exceed 60°C.

The difference between the temperatures in both operation extremes can be explained by twice higher input current in the minimal input voltage case.

V. Technical-Economical Analysis

It is essential to design and build a compact converter with high power density [1, 2]. For that reason dimensions of the discussed capacitors are of essential importance to find the most effective placement. The total volume of one SMD electrolytic capacitor (220 µF) is 4196.6 mm^3, but the volume of one capacitor (220 µF) that consists of 100 SMDs is 2187.5 mm^3. The total volume of 100 ceramic capacitors is almost twice smaller than that of electrolytic capacitors, moreover, ceramic capacitors can be placed in a more flexible way because of their small dimensions.

VI. Conclusions

This paper presents an experimental study of two SMD capacitor types – electrolytic and ceramic.

Operation waveforms in both input voltage extremes showed that no significant visual differences exist in the performance of the two types of capacitors.

Differences in voltage ripple were found in the electrolytic and ceramic capacitor case, especially in the capacitor C_2 case. This fact could be caused by high temperature on the electrolytic capacitors when the voltage ripple damping capability decreases. The heat reduction could be achieved by selecting capacitors with smaller impedance and higher permissible ripple current.

In terms of labour intensity, the mounting of electrolytic capacitors is much more convenient compared to ceramic capacitors.

It can be concluded that if labour intensity and price are not essential, then SMD ceramic capacitors can be recommended for high power applications. Electrolytic capacitors could be implemented only in the case of paralleling them in order to reduce total impedance.

References

[1] J.W. Kolar, U. Drofenik, J. Biela, M.L. Heldwein, H. Ertl, T. Friedli, S.D. Round, " PWM Converter Power Density Barriers," presented at 7th Power Conversion Conference PCC '07, Nagoya, Japan 2007.

[2] F.H. Khan, L.M. Tolbert, "5 kW Multilevel DC-DC Converter for Hybrid Electric and Fuel Cell Automotive Applications," Industry Applications Conference, 42nd IAS Annual Meeting, pp.628-635, 23-27 Sept. 2007.

[3] Yuan Li; J. Anderson, F.Z. Peng, Dichen Liu, "Quasi-Z-Source Inverter for Photovoltaic Power Generation Systems," presented at 24th Applied Power Electronics Conference and Exposition, APEC 2009.

[4] D. Vinnikov, I. Roasto, J. Zakis, R. Strzelecki, "New Step-Up DC/DC Converter for Fuel Cell Powered Distributed Generation Systems: Some Design Guidelines". Journal "Electrical Review" ISSN 0033-2097, vol. 86, nr. 8, pp. 245-252, 2010.

[5] Murata® Technical Bulletin (online). Available: www.murata.com

[6] Panasonic® Technical Bulletin (online). Available: www.panasonic.com

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